# Electronics \& Communications Engineering 

## Model Question Papers

## For Undergraduate Program

The model question papers are suggestive blueprints. The primary aim of these question papers is to bring clarity about the process of connecting questions to performance indicators and hence to course outcomes. Further, these question papers demonstrate how bloom's taxonomy can be used to understand the quality of question papers and their effectiveness in assessing higher order abilities. The structure of question papers, number of questions, choices given, time given for examination etc., can vary based on the practices of the University or college.

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## Course Name: Analog Electronics Circuits

Semester: III (ECE)
Course Outcomes (CO):

1. Infer the terminal behaviour of the devices such as Junction Diode, BJT \&MOSFET, also identify the region of operation with its equivalent circuit model.
2. Identify the need for small signal operation and derive the small signal performance parameters of the device for amplification by relating design variable to the device parameters.
3. Outline and parse the performance parameters of various feedback topologies \& large signal amplifiers.
4. Develop the basic analog functional block for an application, and verify its functionality using a suitable ECAD tool.

# Model Question Paper <br> Total Duration (H: M): 3:00 <br> Course: Analog Electronic Circuits <br> Maximum Marks: 100 

| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
| UNIT I |  |  |  |  |  |
| 1a | Design the following circuit to provide the output voltage $\mathrm{V}_{0}$ of 3.8 V . Assume that the diodes have 0.7 V drop at 1 mA and $\Delta \mathrm{V}=0.1 \mathrm{~V} /$ decade change in current. | 7 | 1 | 3 | 2.1.2 |
| 1b | Derive the DC bias currents $\mathrm{I}_{\mathrm{B}}, \mathrm{I}_{\mathrm{C}}, \mathrm{I}_{\mathrm{E}}, \mathrm{V}_{\mathrm{CE}}$ and $\mathrm{S}_{\mathrm{ICO}}$ for voltage divider biasing using BJT. Draw the DC load line and locate the operating point. With the help of sequence of events show how the operating point is stabilized. | 7 | 1 | 2 | 1.4.2 |
| 1c | Design a circuit using suitable components to obtain the following input- output characteristics and explain the working of the same. | 6 | 1 | 3 | 2.1.2 |
| 2a | The input voltage Vi to the circuit shown below varies linearly from 0 to 150 V . Sketch the output waveform. Assume diodes as ideal. | 7 | 1 | 3 | 2.1.2 |


| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |
| 2b | List different diode models. Explain any three models in detail. | 7 | 1 | 2 | 1.4.2 |
| 2c | Identify the circuit and plot the output waveform if the input signal $\mathrm{V}_{\mathrm{i}}$ shown below is applied. Given $\mathrm{C}=1 \mu \mathrm{~F}, \mathrm{~V}=5 \mathrm{~V}$, cut in voltage of the diode $\mathrm{V}_{\mathrm{Y}}=0.7 \mathrm{~V}$ | 6 | 1 | 3 | 2.1.2 |
| 3 a | Identify the following amplifier configuration and determine the DC bias voltages and currents to locate the Q -point. Compute various amplifier parameters when $\mathrm{R}_{1}=68 \mathrm{k} \Omega, \mathrm{R}_{2}=12 \mathrm{k} \Omega, \mathrm{V}_{\mathrm{CC}}=18 \mathrm{~V}, \mathrm{R}_{\mathrm{C}}=2.2 \mathrm{k} \Omega, \mathrm{R}_{\mathrm{E}}=1.2 \mathrm{k} \Omega$, $\mathrm{h}_{\mathrm{fe}}=180, \mathrm{~h}_{\mathrm{ie}}=2.75 \mathrm{~K} \Omega, \mathrm{~h}_{\mathrm{oe}}=25 \mu \mathrm{mho}$. | 7 | 2 | 3 | 2.1.2 |
| 3b | Prove that $\mathrm{r}_{\mathrm{d}}=\mathrm{nV} V_{T} / \mathrm{I}_{\mathrm{D}}$ for a small signal diode model with necessary circuit diagram and transfer characteristics curve. | 7 | 1 | 2 | 1.4.2 |
| 3c | Draw the steady state output waveform for the following circuit indicating maximum and minimum value of the output. Given $\mathrm{R}_{\mathrm{r}}=2 \mathrm{M} \Omega, \mathrm{R}_{\mathrm{f}}=0 \Omega$ cut-in voltage of diode $=0 \mathrm{~V}$, input voltage is 5 KHz square wave varying between +10 V and -10 V . | 6 | 1 | 3 | 2.1.2 |


| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |
| UNIT II |  |  |  |  |  |
| 4 a | Find the values of circuit elements shown below for given current $\mathrm{I}_{\mathrm{D}}$ of 0.4 mA , $\mathrm{V}_{\mathrm{D}}=0.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{t}}=0.7 \mathrm{~V}, \mu_{\mathrm{n}} \mathrm{C}_{\mathrm{ox}}=100 \mathrm{~mA} / \mathrm{V}^{2}, \mathrm{~L}=1 \mu \mathrm{~m} \& \mathrm{~W}=32 \mu \mathrm{~m} \mathrm{~V}_{\mathrm{DD}}=-\mathrm{V}_{\mathrm{SS}}=2.5 \mathrm{~V}$. Neglect channel length modulation effect. | 7 | 2 | 3 | 1.4.2 |
| 4b | Design the circuit elements as shown in below figure to establish a DC drain current of 0.5 mA . The NMOS is specified to have $\mathrm{V}_{\mathrm{t}}=1 \mathrm{~V}$ and $\mathrm{k}_{\mathrm{n}}{ }^{\prime}(\mathrm{W} / \mathrm{L})=1 \mathrm{~mA} / \mathrm{V}^{2}$ and $\lambda=0$. Calculate the percentage change in the value of $I_{D}$ obtained when the MOSFET is replaced with another MOSFET having same $\mathrm{k}_{\mathrm{n}}{ }^{\prime}(\mathrm{W} / \mathrm{L})$ but $\mathrm{V}_{\mathrm{t}}=1.5 \mathrm{~V}$ $\mathrm{VDD}=15 \mathrm{~V}$ | 7 | 2 | 3 | 2.1.2 |
| 4c | Draw the DC equivalent, AC equivalent and small signal equivalent model for common gate amplifier and derive the expressions for input, output impedance and voltage gain. | 6 | 2 | 3 | 1.4.1 |
| 5a | Derive an expression for drain current $I_{D}$ for NMOS in different regions of operation. | 7 | 1 | 3 | 1.4.2 |
| 5b | Consider common source amplifier with constant current source biasing technique where $\mathrm{V}_{\mathrm{DD}}=-\mathrm{V}_{\mathrm{SS}}=15 \mathrm{~V}$, current $\mathrm{I}=0.5 \mathrm{~mA}, \mathrm{R}_{\mathrm{G}}=4.7 \mathrm{M} \Omega, \mathrm{R}_{\mathrm{D}}=10 \mathrm{~K} \Omega$, $\mathrm{V}_{\mathrm{t}}=1.5 \mathrm{~V}$ and $\mathrm{K}_{\mathrm{n}}{ }^{\prime}(\mathrm{W} / \mathrm{L})=1 \mathrm{~mA} / \mathrm{V}^{2}$. Determine the Q-points and all the amplifier parameters assuming $\mathrm{V}_{\mathrm{A}}=75 \mathrm{~V}$. | 7 | 2 | 3 | 1.4.2 |


| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 5c | Using two transistors $\mathrm{Q}_{1}$ and $\mathrm{Q}_{2}$ having equal lengths but different widths related by $\mathrm{W}_{2} / \mathrm{W}_{1}=5$. Design a circuit that replicates current and obtain $\mathrm{I}=0.5 \mathrm{~mA}$. Let $\mathrm{V}_{\mathrm{DD}}=5 \mathrm{~V}, \mathrm{k}_{\mathrm{n}}{ }^{\prime}(\mathrm{W} / \mathrm{L})_{1}=0.8 \mathrm{~mA} / \mathrm{V}^{2}, \mathrm{~V}_{\mathrm{t}}=1 \mathrm{~V}$ and $\lambda=0$. Find the required value of R ? What is voltage at the gates of $\mathrm{Q}_{1}$ and $\mathrm{Q}_{2}$ ? What is the lowest voltage allowed at the drain of $\mathrm{Q}_{2}$ while $\mathrm{Q}_{2}$ remains in the saturation region? | 6 | 2 | 3 | 2.1.2 |
| 6 a | Explain the working of N -channel enhancement mode MOSFET with relevant diagrams. | 7 | 1 | 2 | 1.4.2 |
| 6b | The NMOS transistors used in the following circuits have $\mathrm{V}_{\mathrm{t}}=1 \mathrm{~V}, \mu_{\mathrm{n}} \mathrm{C}_{\mathrm{ox}}=120$ $\mu \mathrm{A} / \mathrm{V}^{2}, \lambda=0, \mathrm{~L}_{1}=\mathrm{L}_{2}=\mathrm{L}_{3}=1 \mu \mathrm{~m}$. Find the equivalent values of gate widths for each of transistors to obtain voltage values as indicated in the figure and current of $120 \mu \mathrm{~A}$. | 7 | 2 | 3 | 2.1.2 |
| 6 c | A drain current of $115 \mu \mathrm{~A}$ and drain voltage of 3.5 V is to be developed across the MOSFET shown in below figure, obtain the value of R to meet the requirement. Given $\mathrm{V}_{\mathrm{t}}=-0.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{DD}}=5 \mathrm{~V} \mu_{\mathrm{p}} \mathrm{C}_{\mathrm{ox}}=60 \mu \mathrm{~A} / \mathrm{V}^{2}, \mathrm{~L}=0.8 \mu \mathrm{~m}$ and $\lambda=0$. Determine the width of the channel. | 6 | 2 | 3 | 2.1.2 |
| UNIT III |  |  |  |  |  |
| 7 a. | An amplifier with negative feedback has a voltage gain of 120. It is found that without feedback, an input signal of 60 mV is required to produce a particular output. Find the Av and $\beta$ of the amplifier. | 6 | 3 | 2 | 1.4.2 |
| 7b. | Discuss the general characteristics of a negative feedback amplifier. | 6 | 3 | 2 | 1.4.2 |


| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :--- | :---: | :---: | :---: | :---: |
| 7c. | Derive an expression for input and output resistance of a voltage shunt feedback <br> amplifier, and explain. | 8 | 3 | 3 | 1.4 .2 |
| 8a. | Explain the classification of power amplifiers based on the location of the <br> operating point with neat diagrams. | 6 | 3 | 2 | 1.4 .2 |
| 8b. | A class B power amplifier is delivering an output voltage of 10 volts peak to an <br> $8 \Omega$ load, if the DC power supply is 30 volts; calculate i) DC power input. ii) AC <br> power delivered to the load iii) Conversion efficiency iv) Power dissipated in the <br> collector of each transistor. | 6 | 3 | 3 | 1.4 .2 |
| 8c. | A loud speaker with an 8 ohm input resistance requiring a power of 0.5 W is to <br> be driven by the following amplifier configuration. VCC is a 9V battery, and the <br> identical transistors have V <br> for output transformer. | 8 | 3 | 3 | 2.1 .2 |

Blooms Level wise Marks Distrbution

■ Level 2 Level 3



BL - Bloom's Taxonomy Levels (1- Remembering, 2- Understanding, 3 - Applying, 4 Analysing, 5 - Evaluating, 6 - Creating)
CO - Course Outcomes
PO - Program Outcomes; PI Code - Performance Indicator Code

## Course Name: Automotive Electronics

Semester: VI (ECE)
Course Outcomes (CO):

1. Discuss the overview of automotive components, subsystems, design cycles, communication protocols and safety systems employed in today's automotive industry.
2. Determine the role of electronics for the areas like In-vehicle architectures, networking, engine management systems, vehicle safety systems \& infotainment systems.
3. Select, classify and interface sensors to automotive systems.
4. Establish the need of vehicle safety standards and diagnostics systems in the automotive industry and implications on OEMs, Suppliers and Customers.
5. Design and implement an automotive sub system to realize Electronic Control Unit.

> Model Question Paper
> Total Duration (H: M):3:00 Course: Automotive Electronics Maximum Marks: 100

| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
| UNIT I |  |  |  |  |  |
| 1a | The vehicle is to be started on a cold winter morning, and then has to navigate hilly terrains. How does the engine cope-up with the different requirements as the vehicle goes from start to cruising? Suggest a design strategy using different control modes with appropriate details. | 8 | 2 | 3 | 2.1.2 |
| 1 b | What is Stoichiometric ratio? <br> i) Calculate Lambda if air fuel ratio is 13.2. <br> ii) Determine the fuel injector pulse duration (base pulse width Tw) and fuel quantity for the eight cylinder fully warmed up and very cold engine running at 4000 rpm , having a fuel flow rate of $0.0022 \mathrm{Kg} / \mathrm{sec}$ and mass air flow rate of $0.0035 \mathrm{Kg} / \mathrm{sec}$. | 6 | 2 | 3 | 1.4.1 |
| 1c | For the development of an Engine ECU, apply MBD approach adhering to automotive V design model. | 6 | 1 | 3 | 1.4.1 |
| 2a | With MAF sensor malfunctioning as detected by the engine control system diagnostic function, how engine control system can work effectively as possible with other existing sensor information for calculating the mass air flow rate. | 8 | 2 | 3 | 1.4.1 |
| 2b | Assume a vehicle is running at a fixed rpm of 8000 and further the driver demands for increase in speed. How the engine ECU handles driver's request using ignition timing? Suggest a suitable Instrumentation system with related electronics for closed loop control of ignition timing. | 6 | 2 | 3 | 2.2.3 |
| 2c | Vehicle is moving with a high speed; suddenly the driver applies the brakes, what is the physical consequence of this condition on wet and dry surface? Provide a suitable control system/electronic solution to avoid the damage. | 6 | 1 | 3 | 2.2.3 |
| 3 a | What do you mean by Engine Mapping? For the engine operating in closed loop mode how the variations in, <br> i) Exhaust gas recirculation <br> ii) Air fuel ratio and <br> iii) Ignition timing <br> affect its performance. Show with the necessary plots. | 8 | 2 | 2 | 1.4.1 |


| Q.No | Questions | Marks | CO | BL | PI |
| :--- | :--- | :---: | :---: | :---: | :---: |
| 3b | $\begin{array}{l}\text { Elaborate on different segments of automotive industry and also discuss about } \\ \text { automotive supply and value chain. }\end{array}$ | 6 | 1 | 2 | 1.4 .1 |
| 3c | $\begin{array}{l}\text { Vehicle is moving on an icy surface with the engine rpm of 4000, but the vehicle } \\ \text { is unable to move forward, what is the physical consequence of this condition? } \\ \text { Provide a control system solution to overcome this problem. }\end{array}$ | 6 | 1 | 2 | 2.2 .3 |
| UNIT II |  |  |  |  |  |
| 4a | $\begin{array}{l}\text { Describe the control system which provides a solution for wheel spinning, and } \\ \text { discuss the related control functions. Brief on operating sequence of drivers air } \\ \text { bag. }\end{array}$ | 8 | 3 | 2 | 1.4 .1 |
| 4b | $\begin{array}{l}\text { Compare event driven and time triggered communication strategies. Calculate } \\ \text { nominal and maximum THeader ,TRespone and T Trame, if LIN is operating at 10Kbps } \\ \text { baud rate and reserved time is set to 30\% for transmitting two bytes of data. }\end{array}$ | 6 | 2 | 3 | 2.1 .2 |
| 4c | $\begin{array}{l}\text { What is ride and handling of an automobile? How electronic suspension system } \\ \text { manages the compromise between ride comfort and handling. }\end{array}$ | 6 | 3 | 2 | 1.4 .1 |
| 5a | $\begin{array}{l}\text { Discuss the physical mechanism of wheel lock and vehicle skid that can occur } \\ \text { during braking; How the ABS configuration provides a solution for this. If the } \\ \text { vehicle longitudinal acceleration is zero, } \\ \text { i) Calculate the wheel slip if vehicle speed is matching with wheel speed? } \\ \text { ii) Calculate wheel slip for Fl(Front left) and Fr(Front right), when vehicle speed }\end{array}$ | 8 | 3 | 3 | 1.4 .1 |
| is 70kph and WssFl(Wheel speed front left) and WssFr(Wheel speed front right) |  |  |  |  |  |$)$


| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |
| 6b | Explain the construction and working principle of magnetic reluctance angular position sensor. What is the drawback of this sensor and how it is overcome? Discuss the operation of fuel injector. | 6 | 3 | 2 | 1.4.1 |
| 6c | The fast moving car is turning at the corner, if the vehicle is turning less/more than the driver's intention suggest a suitable control system along with the break circuit configuration to overcome this condition. | 6 | 3 | 3 | 2.1.2 |
| UNIT III |  |  |  |  |  |
| 7 a | For an electric vehicle propulsion system the hazardous event is described as "Un intended vehicle acceleration during a low speed maneuver amongst pedestrians". Perform suitable hazard analysis and risk assessment for this case. | 10 | 3 | 3 | 2.1.2 |
| 7b | An engine going through cold cranking the air/fuel ratio is not able to be controlled. Analyze the possible faults. | 10 | 3 | 2 | 1.4.1 |
| 8 a | The CAN node has to transmit the speed sensor information from engine ECU to ESP ECU. The size of the information of 5 bits, show how this message is transmitted, and discusses how the CAN receiver node determines whether the message is error free or not. | 10 | 4 | 3 | 1.4.1 |
| 8b | A 2015 Audi A8 was having a problem with rough running which in turn was causing the engine management light to illuminate. Analyze the possible faults | 10 | 4 | 3 | 2.1.2 |




BL - Bloom's Taxonomy Levels (1- Remembering, 2- Understanding, 3 - Applying, 4 Analysing, 5 - Evaluating, 6 - Creating)
CO - Course Outcomes
PO - Program Outcomes; PI Code - Performance Indicator Code

## Course Name: CMOS VLSI Circuits

Semester: V (ECE)
Course Outcomes (CO):
6. Illustrate the CMOS VLSI design flow and Outline the CMOS IC fabrication process
7. Model the DC Characteristics and delays of CMOS logic circuits.
8. Design complex CMOS logic circuits using stick diagrams \& interpret layout design rules.
9. Design combinational and sequential CMOS logic networks.
10. Analyze and interpret the static and transient performance of logic gates and verify layouts using Cadence tool.
11. Design and analyze combinational and sequential logic circuits using Cadence tool.

> Model Question Paper
> Total Duration (H:M): 3:00
> Course: CMOS VLSI Circuits

Maximum Marks :100

| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
| UNIT I |  |  |  |  |  |
| 1a | Analyze the impact of Semi-custom and Full-custom VLSI design styles based on design cycle time and the achievable circuit performance. | 6 | 1 | 2 | 1.4.2 |
| 1b | What are the limitations of planar VLSI technology, and discuss the advantages and challenges in 3D devices like FinFET devices. | 6 | 1 | 2 | 1.2.1 |
| 1c | In VLSI fabrication, oxides in varying thickness and compositions are used for different processes. Discuss each of them with relevant examples. | 8 | 1 | 2 | 1.2.3 |
| 2a | Discuss the capacitance modeling of an nMOS device during cutoff, linear and saturation. | 6 | 2 | 2 | 1.4.1 |
| 2b | Design an AOI221 gate using fully CMOS logic, so as to achieve same transient performance as that of a reference CMOS Inverter. | 6 | 2 | 3 | 14.2.2 |
| 2c | Solve the node voltages in the arrangements given below if $\mathrm{V}_{\mathrm{tn}}=0.6 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{tp}}=$ -0.6 V . What may happen to the output voltage, if the back-gate effect is also considered? | 8 | 2 | 3 | 1.4.1 |
| 3 a | An inverter needs to be fabricated using planar CMOS technology in a twin-tub process. Illustrate the fabrication steps with cross-sectional views and appropriate masks used at each stage. | 10 | 1 | 3 | 1.2.1 |


| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 3 b | A circuit designer has a choice to implement combinational logic using NAND or a NOR network. Justify the selection if performance is the criteria, and analyze the speed of a 1 to 0 transition as shown below. <br> The output cap has a value of $\mathrm{C}_{\text {out }}=130 \mathrm{fF}$, while the internal values are $\mathrm{C}_{1}=\mathrm{C}_{2}=36 \mathrm{fF}$. The transistors are identical with $\beta_{\mathrm{n}}=2.0 \mathrm{~mA} / \mathrm{V}^{2}$ in a process where $\mathrm{V}_{\mathrm{DD}}=3.3 \mathrm{~V} \& \mathrm{~V}_{\mathrm{Tn}}=0.7 \mathrm{~V}$. <br> i. Find the discharge time constant for $\mathrm{C}_{\text {out }}=130 \mathrm{fF}$ using the ladder RC network. <br> ii. Find the time constant if we ignore $\mathrm{C}_{1} \& \mathrm{C}_{2}$. <br> iii. What is the percentage error introduced if we do not include the internal capacitors? | 10 | 2 | 3 | 2.1.2 |
| UNIT II |  |  |  |  |  |
| 4a | Discuss the phenomenon of latch-up and illustrate ways of dealing with it in CMOS VLSI design. | 6 | 3 | 2 | 1.4.2 |
| 4b | What is the need to study $\lambda$-based design rules? How are they different from micron rules? Illustrate $\lambda$-based design rules with an example layout. | 6 | 3 | 3 | 14.2.2 |
| 4c | Identify the circuit from the layout given below. Is it a valid layout? If yes then what is the type of logic style it represents? metal-1 diffusion poly <br> - contact n-well | 8 | 3 | 3 | 2.1.2 |
| 5a | Discuss the charge sharing issue in Dynamic CMOS logic. What will happen if we directly cascade two stages of this gate? Propose a remedy for the cascading problem. | 6 | 4 | 3 | 14.2.2 |
| 5b | In the figure, find the output in terms of inputs A, B and C when the clock CK is high. Also implement the clocked CMOS equivalent of the same. | 6 | 4 | 3 | 1.4.2 |


| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |
| 5c | Consider the logic cascade shown in figure below .Use logical effort to find the relative size of each stage needed to minimize delay through the chain. Assume symmetric gates with $\mathrm{r}=2.5$. | 8 | 4 | 3 | 1.4.2 |
| 6 a | For the given logical expression for $Z=\overline{A(D+E)+B C}$ design a suitable logic circuit using CMOS with stick-diagram layout, and optimize the ordering of poly gates in the layout by using appropriate method. | 10 | 3 | 3 | 14.2.2 |
| 6 b | Consider the logic chain of a co-processor shown below. The input at A is switched from a 1 to 0 . Find an expression for the delay time through the chain using an appropriate procedure. | 10 | 4 | 3 | 2.1.2 |
| UNIT III |  |  |  |  |  |
| 7a | Illustrate the flip-flop min-delay constraint with appropriate waveforms and equations. | 10 | 4 | 3 | 1.4.2 |
| 7b | Explain the working of a standard CMOS flip-flop using TGs. | 10 | 4 | 2 | 1.4.2 |
| 8a | A simple latch can be implemented using one MOS device. Discuss the variations and design improvements that can be made based on logic requirements. | 10 | 4 | 3 | 1.4.2 |


| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :--- | :---: | :---: | :---: | :--- |
| 8 b | Write a short note on Global clock-generation and distribution | 10 | 4 | 2 | 1.4 .2 |




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CO - Course Outcomes
PO - Program Outcomes; PI Code - Performance Indicator Code

## Course Name: Digital Circuits

## Semester: III (ECE)

Course Outcomes (CO):

1. Evaluate the performance metrics of digital circuits.
2. Design a combinational circuit using Medium Scale Integration (MSI) devices by applying suitable reduction techniques.
3. Design a sequential circuit using Flip Flops.
4. Illustrate the role of different types of memories in computer system.
5. Design \& implement combinational/sequential logic system for a given application to meet the functional requirements.

Model Question Paper
Total Duration (H: M): 3:00
Course: Digital Circuits
Maximum Marks: 100

| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
| UNIT I |  |  |  |  |  |
| 1a | Explain the working of ECL OR gate with the help of neat circuit diagram. | 5 | 1 | 2 | 1.4.2 |
| 1b | Rewrite the following Boolean expression in the minterm and maxterm canonical forms. $P=F(x, y, z)=x^{\prime}\left(y^{\prime}+z\right)+z^{\prime}$ | 5 | 2 | 2 | 1.4.1 |
| 1c | Design a digital circuit using minterm and maxterm generators to realize the following functionality. $\mathrm{F}(\mathrm{~A}, \mathrm{~B}, \mathrm{C}, \mathrm{D})=\Sigma \mathrm{m}(0,1,3,4,9,10,11,15) .$ <br> Use only 2 - input gates. | 10 | 2 | 3 | 2.2.3 |
| 2a | On a certain weekend Ramu, Raheem and Johnny planned to have lunch in a restaurant and/or watch a movie. <br> i) When all friends agree, they will have lunch after watching a movie. <br> ii) No question of going out when none of them agree. <br> iii) If Ramu agrees, then irrespective of others opinion, they only have lunch together. <br> iv) If Ramu disagrees, they will only watch a movie. <br> Design a suitable digital system by using a positive logic, for the above conditions with a non programmable technique in SOP and POS formats. | 10 | 2 | 3 | 2.2.3 |
| 2b | Realize the following Boolean function with multiplexer $\mathrm{F}(\mathrm{~A}, \mathrm{~B}, \mathrm{C}, \mathrm{D})=\sum \mathrm{m}(0,1,3,4,8,9,15)$ <br> i) Using 16:1 MUX <br> ii) Using 8:1 MUX with $\mathrm{A}, \mathrm{B}, \mathrm{C}$ select lines <br> iii) Using 4:1 MUX with A,B select lines | 10 | 2 | 3 | 1.4.1 |
| 3a | Identify a technique that cannot be programmed and that is used for less number of variables, to provide minimal sums and minimal products for the following Boolean function. $\mathrm{f}(\mathrm{w}, \mathrm{x}, \mathrm{y}, \mathrm{z})=\sum \mathrm{m}(1,5,8,14)+\mathrm{X}(4,6,9,11,15)$ | 10 | 2 | 3 | 2.2.3 |


| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 3b | Design a digital system to add two Binary Coded Decimal numbers using binary adder. | 10 | 2 | 3 | 1.4.1 |
| UNIT II |  |  |  |  |  |
| 4a | Explain the operation of a SR latch. | 7 | 3 | 2 | 1.4.2 |
| 4b | Design a 4-bit Johnson counter using the principle of Universal Shift Register (USR) | 7 | 3 | 3 | 1.4.1 |
| 4 c | The figure shows a binary up counter with synchronous clear input. With the decoding logic shown, the counter works as a Mod-n counter. Find the value of n. | 6 | 3 | 3 | 1.4.2 |
| 5a | What is race around condition? Explain the remedy for the same problem in case of JK F/F. | 7 | 3 | 2 | 1.4.2 |
| 5b | Design a digital system using minimum number of data flip flops to monitor the number of buses available in the bus depot on daily basis for the following conditions, over a week. <br> - On Sunday the occupancy of bus depot is 15 buses. <br> - On Monday 2 buses were sent for service. <br> - On Tuesday 3 buses went for college trip. <br> - On Wednesday 1 bus returned from service. <br> - Next day 5 more buses left for marriage party. <br> - On Friday buses returned from college trip. <br> - On Saturday 2 buses were sent for service. | 7 | 3 | 3 | 2.2.2 |
| 5c | Five JK flip-flops are cascaded to form the circuit shown in figure. Clock pulses at a frequency of 1 MHz are applied as shown. Compute the frequency (in KHz) of the wave form at Q3. | 6 | 3 | 3 | 1.4.2 |
| 6a | Analyze a negative edge triggered D Flip-Flop with the help of timing diagram. | 7 | 3 | 3 | 1.4.2 |


| Q.No | Questions |  |  |  |  | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 6b | Design a digital system using suitable logic to count from $(0010)_{2}$ till it reaches $(1101)_{2}$ continuously. The external clock is given to the first Flip-Flop and triggers it during rising edge of the pulse. The successive Flip-Flops are to be triggered by its predecessors. |  |  |  |  | 7 | 3 | 3 | 2.2.2 |
| 6 c | A three bit pseudo random generator is as shown. Initially the value of output $\mathrm{Y}=\mathrm{Y}_{2} \mathrm{Y}_{1} \mathrm{Y}_{0}$ is set to 111 . Evaluate the value of output Y after three clock cycles. |  |  |  |  | 6 | 3 | 3 | 1.4.2 |
| UNIT III |  |  |  |  |  |  |  |  |  |
| 7 a | Draw Mealy and Moore synchronous machine models and label the excitation variables, state variables, input and output variables. |  |  |  |  | 10 | 3 | 2 | 1.4.2 |
| 7b | Design a digital c component with si | r for <br> put. <br> ate <br> B <br> 0 <br> 1 <br> 0 <br> 1 <br> 0 <br> 1 <br> 0 <br> 1 | tate ta <br> Input <br> $X$ <br> 0 <br> 0 <br> 1 <br> 1 <br> 0 <br> 0 <br> 1 | ven <br>  <br> N <br> A <br>  <br> 0 <br> 0 <br> 1 <br> 1 <br> 0 <br> 1 <br> 1 <br> 1 <br> 0 | using a sequential | 10 | 3 | 3 | 2.2.3 |
| 8a | Differentiate between SRAM, DRAM, NVRAM. |  |  |  |  | 10 | 4 | 2 | 1.4.1 |
| 8b | Explain the read and write operations of SRAM. |  |  |  |  | 10 | 4 | 2 | 1.4.1 |




BL - Bloom's Taxonomy Levels (1- Remembering, 2- Understanding, 3 - Applying, 4 Analysing, 5 - Evaluating, 6 - Creating)
CO - Course Outcomes
PO - Program Outcomes; PI Code - Performance Indicator Code

## Course Name: Linear Integrated Circuits

Semester: IV (ECE)
Course Outcomes (CO):

1. Describe the operation of current mirror, differential Amplifier using MOSFET and analyze the respective performance parameters.
2. Design and analyze the operations of linear applications using Op-amp for the given specifications.
3. Design and analyze the operations of non-linear applications using Op-amp for the given specification.
4. Realize the functional block for a given application and specifications using op-amp and linear ICs and verify its functionality using simulator tool.

# Model Question Paper <br> Total Duration (H: M):3:00 <br> Course: Linear Integrated Circuits 

Maximum Marks: 100

| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
| UNIT I |  |  |  |  |  |
| 1a | Derive the expression for output impedance of Wilson current mirror with relevant circuit diagram and equivalent circuits. | 6 | 1 | 3 | 1.4.2 |
| 1b | For the non inverting amplifier $\mathrm{R}_{1}=470 \Omega$ and $\mathrm{R}_{\mathrm{F}}=4.7 \mathrm{~K} \Omega, \mathrm{~A}=200000, \mathrm{R}_{\mathrm{i}}=2 \mathrm{M} \Omega$, $\mathrm{R}_{0}=75 \mathrm{~F}_{\mathrm{o}}=5 \mathrm{~Hz}$, supply voltage is $+/-15 \mathrm{~V}$ and output voltage swing is $+/-13 \mathrm{~V}$ Calculate the values of $\mathrm{A}_{\mathrm{F}}, \mathrm{R}_{\mathrm{if}}$. $\mathrm{R}_{\mathrm{of}}, \mathrm{F}_{\mathrm{f}}$ and $\mathrm{V}_{\mathrm{oot}}$ | 6 | 1 | 2 | 1.4.2 |
| 1c | Consider the circuit shown below, assuming <br> $(\mathrm{W} / \mathrm{L})_{1-3}=40 / 0.5$, Iref $=0.3 \mathrm{~mA}$ <br> a. Determine $\mathrm{V}_{\mathrm{b}}$ such that $\mathrm{Vx}=\mathrm{Vy}$ <br> b. If $\mathrm{V}_{\mathrm{b}}$ deviates from the value calculated in part (a) by 100 mV , what is the mismatch between $\mathrm{I}_{\text {out }}$ and $\mathrm{I}_{\mathrm{ref}}$ ? | 8 | 1 | 3 | 2.1.2 |
| 2a | Derive an output voltage expression for 5-pack differential amplifier with neat circuit diagram with relevant Explanation. | 6 | 1 | 3 | 1.4.2 |
| 2b | Discuss the effect of negative feedback on non-idealities of the Op-amp, with neat diagram and relevant equations. | 6 | 1 | 2 | 1.4.1 |
| 2c | Identify the circuit shown below where all transistors have $\mathrm{V}_{\mathrm{t}}=0,6 \mathrm{~V}, \mu_{\mathrm{n}} \mathrm{C}_{\mathrm{ox}}=160$ $\mathrm{W}_{1}=\mathrm{W}_{4}=4 \mu \mathrm{~m}$, and $\mathrm{W}_{2}=\mathrm{W}_{3}=40 \mu \mathrm{~m}$. $\mathrm{L}=1 \mu \mathrm{~m}$ and $\mathrm{I}_{\text {ReF }}$ is $20 \mu \mathrm{~A}$. Determine the | 8 | 1 | 3 | 2.1.2 |


| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | output current and the voltages at the gates of $\mathrm{Q}_{2}$ and $\mathrm{Q}_{3}$. What is the lowest voltage at the output for which current source operation is possible? What are the values of gm and $\mathrm{r}_{0}$ of $\mathrm{Q}_{2}$ and $\mathrm{Q}_{3}$ ? What is the output resistance of the circuit? |  |  |  |  |
| 3 a | Identify the amplifier configuration given below, with $(\mathrm{W} / \mathrm{L})_{1,2}=25 / 0.5$, $\mu_{\mathrm{n}} \mathrm{C}_{\mathrm{ox}}=50 \mu \mathrm{~A} / \mathrm{V}^{2}, \mathrm{~V}_{\mathrm{TH}}=0.6 \mathrm{~V}, \lambda=\gamma=0$ and $\mathrm{V}_{\mathrm{DD}}=3 \mathrm{~V}$ <br> a. What is the required input CM for which $\mathrm{R}_{\text {SS }}$ sustains 0.5 V ? <br> b. Calculate $\mathrm{R}_{\mathrm{D}}$ for a differential gain of 5 | 6 | 1 | 3 | 2.1.2 |
| 3b | List the ideal characteristics of an OPAMP. Give its symbolical representation and explain the functions of each terminal. Tabulate the ideal op-amp terminal characteristics. | 6 | 1 | 2 | 1.4.2 |
| 3 c | For the differential amplifier with the current mirror as a load ,determine the (W/L) and drain current of all MOSFET's for the following specifications: <br> Vdd $=-\mathrm{Vss}=2.5 \mathrm{~V}, \mathrm{SR}>=10 \mathrm{~V} / \mathrm{us} \quad\left(\mathrm{C}_{\text {load }}=5 \mathrm{pf}\right), \mathrm{f}-$ - ab $>=100 \mathrm{kHz} \quad(\mathrm{CL}=5 \mathrm{pF})$,a small signal voltage gain of $100,-1.5<=\mathrm{ICMR}<=2 \mathrm{~V}$ and $\mathrm{P}_{\text {diss }}<=1 \mathrm{~mW}$. Model parameters: $\mathrm{K}_{\mathrm{N}}{ }^{\prime}=110 \mathrm{uA} / \mathrm{V}^{2,} \mathrm{~K}_{\mathrm{P}}{ }^{\prime}=50 \mathrm{uA} / \mathrm{V}^{2,} \mathrm{~V}_{\mathrm{TP}}=-0.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{TN}}=0.7 \mathrm{~V}, \lambda \mathrm{~N}=0.04 \mathrm{~V}^{-}$ ${ }^{1}, \lambda_{P}=0.05 \mathrm{~V}^{-1}$. | 8 | 1 | 3 | 1.4.1 |
| UNIT II |  |  |  |  |  |
| 4a | Derive the expression for the output current Io in terms of input voltage Vin for a grounded load using Op-amp. | 7 | 2 | 3 | 1.4.2 |
| 4b | Describe the inverting differentiator and obtain the expression for the output voltage with neat circuit diagram and waveforms | 7 | 2 | 3 | 1.4.2 |
| 4 c | Identify the following circuit operation. Find | 6 | 2 | 3 | 1.4.2 |


| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | 1. Lower frequency limit of the operation and <br> 2. Response for the step, square and sine inputs for $\mathrm{R}_{1}=10 \mathrm{~K} \Omega, \mathrm{R}_{\mathrm{f}}=100 \mathrm{~K} \Omega$ and $\mathrm{C}_{\mathrm{f}}=1 \mathrm{nF}$ |  |  |  |  |
| 5a | Derive the expression for summing and averaging amplifier output for <br> - Non-inverting amplifier <br> - Differential amplifier <br> Using Op-amp with neat circuit diagram. | 7 | 2 | 3 | 1.4.2 |
| 5b | Two different pre-amp microphones are used in a recording studio, one for vocals and other for the musical instrument with output voltage in the range of $0-2 \mathrm{~V}$ and $0-0.5 \mathrm{~V}$ respectively. Design a suitable circuit using Op-Amp to combine signals from both the microphones in such a way that the signal corresponding to the musical instrument should be twice amplified as that of vocal signal. | 7 | 2 | 3 | 2.1.2 |
| 5c | i. Find $V_{N}, V_{P}$ and $V_{o}$ in the circuit if $V_{s}=9 \mathrm{~V}$ <br> ii. Find the resistance $R$ that, if connected between the inverting input pin of the op-amp and ground which causes Vo to double. | 6 | 2 | 3 | 1.4.2 |
| 6a | Obtain the output expression using a suitable circuit to get the following waveform $\mathrm{Z}(\mathrm{t})$ at the output side. Explain with the help of frequency response. | 7 | 1 | 2 | 1.4.2 |


| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 6b | It is required to measure the weight of the vehicle using weigh bridge system, arrive at a suitable signal conditioning circuit for measuring the weight in terms of voltage. Using circuit analysis techniques arrive at an expression for the output voltage in terms of input weight. | 7 | 1 | 3 | 2.1.2 |
| 6c | Obtain a suitable circuit for the following frequency response with $\mathrm{A}_{\mathrm{F}}=10, \mathrm{f}_{\mathrm{H}}$ and also derive the expression for the gain $A_{F}$ and cut off frequency $f_{H}$ | 6 | 2 | 3 | 2.1.2 |
| UNIT III |  |  |  |  |  |
| 7 a . | Design a circuit using Op-Amp to obtain the following transfer characteristics. Explain the operation using waveforms and obtain the expressions. $\mathrm{V}_{\text {LTP }}=-2$; $\mathrm{V}_{\mathrm{UTP}}=3 ; \mathrm{V}_{\mathrm{SAT}}=15 ;-\mathrm{V}_{\mathrm{SAT}}=15$. | 10 | 3 | 3 | 2.1.2 |
| 7 b . | Draw the circuit configuration to generate triangular wave, describe the circuit operation using waveforms. | 10 | 3 | 2 | 1.4.2 |
| 8 a. | Implement a monostable multivibrator using the timer circuit shown in below figure. Also determine an expression for ON time ' T ' of the output pulse. | 10 | 3 | 3 | 1.4.2 |
| 8 b . | Explain the precision peak detector and precision clamping circuit with neat diagrams. | 10 | 3 | 2 | 1.4.2 |




BL - Bloom's Taxonomy Levels (1- Remembering, 2- Understanding, 3 - Applying, 4 Analysing, 5 - Evaluating, 6 - Creating)
CO - Course Outcomes
PO - Program Outcomes; PI Code - Performance Indicator Code

## Course Name: Operating System and Embedded Systems

Semester: V (ECE)
Course Outcomes (CO):
12. Discuss the core structure and functionality of operating system and Real-time Operating system.
13. Study and analyze various algorithms related to process management and resource management.
14. Discuss the various Kernel objects used to achieve task synchronization and communication.
15. Discuss the concepts of embedded system, their classification and categorize the components of typical embedded systems.
16. Develop an embedded application for given specification with hardware and software requirements

## Model Question Paper <br> Total Duration (H:M): 3:00 <br> Course: Operating System and Embedded Systems <br> Maximum Marks :100

| Q.No | Questions |  |  |  | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| UNIT I |  |  |  |  |  |  |  |  |
| 1a | Calculate the average wait time \& TAT for following processes using <br> - SJF (pre-emptive \& non-pre-emptive), <br> - Priority scheduling <br> - RR <br> Compare their performance. |  |  |  | 8 | 2 | 3 | 1.4.5 |
| 1b |  |  |  |  | 6 | 3 | 3 | 2.2.3 |


| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\text { else \{ \}}$ |  |  |  |  |
| 1c | Suppose computer system hardware is to be operated without an OS, discuss the scenario of using this computer for running an application in which password authentication is to be made. Discuss disadvantages of a computer without an OS. Elaborate on the role of OS and its functions. | 6 | 1 | 2 | 1.4.3 |
| 2a | Under what circumstances is rate-monotonic scheduling inferior to earliest-deadline-first scheduling in meeting the deadlines associated with processes? <br> Consider the following activities of a car control system. <br> 1. $\mathrm{C}=$ worst case execution time <br> 2. $\mathrm{T}=$ (sampling) period <br> 3. $D=$ deadline <br> Speed measurement: $C=4 \mathrm{~ms}, \mathrm{~T}=20 \mathrm{~ms}, \mathrm{D}=20 \mathrm{~ms}$ <br> ABS control: $\mathrm{C}=10 \mathrm{~ms}, \mathrm{~T}=40 \mathrm{~ms}, \mathrm{D}=40 \mathrm{~ms}$ <br> Fuel injection: $C=40 \mathrm{~ms}, \mathrm{~T}=80 \mathrm{~ms}, \mathrm{D}=80 \mathrm{~ms}$ <br> Try any of the two methods to schedule the tasks. | 8 | 2 | 3 | 2.2.3 |
| 2b | In a multiprogramming and time sharing environment, several users share the system simultaneously. Discuss the security problems that may arise in the situation. Assess the degree of security that can be achieved in both the cases. | 6 | 3 | 2 | 1.4.3 |
| 2c | It is required to generate a student's register enrolled for engineering course in alphabetical order to distribute student's ID. <br> Develop a code using <br> i. Inline assembly <br> ii. Mixed assembly <br> comment on the performance w.r.t time and memory using appropriate optimization technique | 6 | 1 | 3 | 2.2.3 |
| 3 a | Convert the algorithm given in flowchart into <br> 1) "Normal" assembler, where only branches can be conditional. <br> 2) ARM assembler, where all instructions are conditional. <br> 3) Develop 'C' code with optimization <br> 4) Comment on performance w.r.t 1, 2 and 3 | 8 | 3 | 3 | 2.2.3 |
| 3 b | Construct a simple "for loop" in C which operates on an array element in each iteration. Then rewrite the code using suitable loop optimization techniques. Comment on the performance. | 6 | 1 | 3 | 1.4.3 |
| 3 c | An Operating system's PID manager is responsible for managing process identifiers. A unique ID is assigned to the process when it is first created. Discuss how this PID is managed using PCB. Elaborate on process and PCB. | 6 | 2 | 2 | 1.4.3 |


| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
| UNIT II |  |  |  |  |  |
| 4a | Write a code for the scenario where an application needs to perform division operation and display the result on a serial port <br> i. Whenever the divisor is found to be zero, message to be displayed is "division error" <br> ii. Whenever the divisor is smaller than zero, message to be displayed is "underflow error". | 8 | 2 | 3 | 2.2.3 |
| 4b | An automotive company claims that the active suspension components in its newest vehicles analyze and respond to road conditions for every 2.5 cm at 100 kilometers per hour ( 1 inch of highway travel at 60 mph ). Develop a prototype C code by applying RTOS concepts to realize the above scenario. | 6 | 3 | 3 | 1.4.3 |
| 4c | Write an application to measure the time taken to execute the "for loop" <br> i) With "loop unrolling" <br> ii) Without "loop unrolling" <br> Both loops are part of two different tasks. Display the time using serial port. | 6 | 1 | 3 | 1.4.5 |
| 5a | Write an optimized code to create two applications: <br> i. "App1" to convert analog to digital data and store the result in memory pool, <br> ii. "App2" to use this information and display on serial port. Demonstrate optimization with code profiling. | 8 | 2 | 3 | 2.2.3 |
| 5b | What are the different means of achieving multitasking? Explain with suitable examples. | 6 | 3 | 2 | 1.4.3 |
| 5c | Develop a prototype C code by applying RTOS concepts to realize the simple vending machine. The vending machine will sell bottles for $\$ 75$. Customers can enter either a dollar or quarters. Once sufficient amount of money is entered, the vending machine will dispense a bottle of water. If user enters a dollar it will return one quarter in change. <br> A Money Receiver detects the total money entered. The bottle dispenser system holds the water bottles and releases one bottle when the input signal is asserted. A coin return system holds quarters for change and will release one quarter when input is dollar. The money receiver will reject money if a dollar and quarter are entered simultaneously. | 6 | 1 | 3 | 2.2.3 |
| 6a | Write a code to create 3 applications, where they share stepper motor: <br> i. "App1" rotates stepper motor in clockwise for 5 rotations <br> ii. "App2" rotates it in anticlockwise for 5 rotations <br> iii. "App3" stops it for one second (use hardware timer) | 8 | 3 | 3 | 2.2.3 |
| 6b | Consider a machine with 64 MB physical memory and a 32 -bit virtual address space. If the page size is 4 KB , what is the approximate size of the page table? Explain the steps with neat diagrams. | 6 | 1 | 2 | 1.4.3 |
| 6c | Two analog sensors are connected to INT0 \& INT1 to monitor blood pressure and body temperature respectively. It is required to generate an alarm if any of the readings exceed the set threshold value. Identify the number of tasks, kernel objects and scheduling algorithm required to handle this situation. Develop a code to demonstrate the same. | 6 | 2 | 3 | 1.4.5 |
| UNIT III |  |  |  |  |  |
| 7 a | Consider a 2M-pixel digital camera with 24 bits per pixel, 8 Mbytes of memory, and a 128 -Mbyte flash card. Assuming computation is instantaneous, with a $10-$ | 10 | 3 | 3 | 2.2.3 |


| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :--- | :---: | :---: | :---: | :---: |
|  | ns word-addressed memory, how many pictures per minute can you take, and <br> after how many pictures does the camera stop writing pictures to the flash? How <br> does this change for a 3M-pixel digital camera with all other parameters <br> remaining the same? |  |  |  |  |
| 7b | Why is backward compatibility less important in an embedded device than in a <br> general-purpose device? In what ways it is still important? | 10 | 3 | 2 | 1.4 .3 |
| 8a | Explain the advantages of wireless devices. How do wireless devices network <br> using different protocol? | 10 | 4 | 2 | 1.4 .3 |
| 8b | Develop a C code to program RTC to generate HOURS, MINUTES and <br> SECONDS using I2C protocol. | 10 | 4 | 3 | 1.4 .5 |



BL - Bloom's Taxonomy Levels (1- Remembering, 2- Understanding, 3 - Applying, 4 - Analysing, 5 Evaluating, 6 - Creating)
CO - Course Outcomes
PO - Program Outcomes; PI Code - Performance Indicator Code

## Course Name: Signals and Systems

Semester: III (ECE)
Course Outcomes (CO):

1. Identify different signals and systems and state their properties both in Continuous and discrete domain.
2. Apply the concept of impulse response and perform convolution in both Continuous and discrete domain to analyze the linear time invariant systems.
3. Perform spectral analysis of discrete time periodic and aperiodic signals using Fourier series, Fourier transform and Z transform techniques.
4. Perform the transformations on a given signal and identify appropriate operations.

Model Question Paper
Total Duration (H: M): 3:00
Course: Signals and Systems
Maximum Marks: 100

| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
| UNIT I |  |  |  |  |  |
| 1 a | Categorize the following signal in terms of energy or power and compute its value. | 6 | 1 | 2 | 1.1.3 |
| 1 b | Obtain the response and sketch the output of the system for the signals $\mathrm{x}_{1}(\mathrm{n})=0.5$ $[\mathrm{u}(\mathrm{n})-\mathrm{u}(\mathrm{n}-3)]$ and $\mathrm{x}_{2}(\mathrm{n})=\mathrm{u}[\mathrm{n}]-\mathrm{u}[\mathrm{n}-2]$. | 8 | 2 | 3 | 2.1.2 |
| 1c | Consider the system shown below; determine whether it is (a) memory less (b) Causal (c) linear (d) time-invariant or (e) Stable. | 6 | 1 | 3 | 1.1.3 |
| 2a | For given signals $x(n)$ and $h(n)$ compute the interaction between signal and the impulse response of a system. $x(n)=\{1,3,-1,4\} \quad h(n)=\{4,-1,2\}$ | 6 | 1 | 3 | 2.1.2 |
| 2b | A Continuous-time signal $\mathrm{x}[\mathrm{t}]$ is shown in figure below. Sketch each of the following signals. <br> a) $x[t-4]$ <br> b) $x[3 t+7]$ <br> c) $x[-1(t+2)]$ <br> d) $x[-t+2]$ | 8 | 1 | 2 | 1.1.3 |


| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |
| 2c | Construct signal $\mathrm{x}(\mathrm{t})$ using suitable elementary signals. Express $\mathrm{x}(\mathrm{t})$ in terms of the same. | 6 | 1 | 3 | 2.1.2 |
| 3a | Determine whether the discrete-time signal $\mathbf{x}(\mathbf{n})=\boldsymbol{\operatorname { s i n }}\left(\frac{1}{\mathbf{3}} \boldsymbol{\pi} \boldsymbol{n}\right) \boldsymbol{\operatorname { c o s }}\left(\frac{\mathbf{1}}{\mathbf{5}} \boldsymbol{\pi} \boldsymbol{n}\right)$ is periodic. If periodic, find the fundamental period. | 6 | 1 | 2 | 1.1.3 |
| 3b | Consider the signals $h(t)=[u(t)-u(t-1)]$ and $x(t)$ shown below. Obtain the response of the system. | 8 | 2 | 3 | 2.1.4 |
| 3 c | Sketch the Direct form I implementation for the difference equation, $y(n)-\frac{1}{4} y(n-1)+\frac{1}{8} y(n-2)=x(n)+\frac{1}{2} x(n-2)$ <br> And also propose a solution to implement the difference equation with minimum number of hardware and also sketch the same. | 6 | 2 | 3 | 1.1.3 |
| UNIT II |  |  |  |  |  |
| 4a | Prove the following properties of DTFT <br> a) Frequency Differentiation Property <br> b) Time shift property. | 6 | 3 | 2 | 1.1.3 |
| 4b | Using appropriate transformation compute the frequency response of the following time domain signal shown below. Plot the magnitude and phase spectrum. Also Verify Parseval's identity. | 8 | 4 | 3 | 2.1.4 |


| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |
| 4 c | Obtain the frequency response of the LTI system described the impulse response <br> a) $h(n)=1 / 8(7 / 8)^{n} \cdot u(n)$ <br> b) $h(t)=\delta(t)-2 e^{-2 t} \cdot u(t)$ | 6 | 4 | 3 | 1.1.3 |
| 5a | Using appropriate transformation compute the frequency response of the following time domain signal: $x(n)=(1 / 2)^{n} \cdot\{u(n+3)-u(n-2)\}$ | 6 | 3 | 3 | 2.1.4 |
| 5b | Obtain the impulse response of the system having the input $x(n)=(1 / 2)^{n} \cdot u(n)$ and output $y(n)=1 / 4(1 / 2)^{n} \cdot u(n-1)+(1 / 4)^{n} \cdot u(n) .$ | 8 | 3 | 3 | 2.1.2 |
| 5c | Prove the following properties of DTFS <br> a) Convolution Property <br> b) Linearity property. | 6 | 3 | 2 | 1.1.3 |
| 6a | Using appropriate transformation find and sketch the time domain signal corresponding to the following Fourier representation. $X(k)=2+2 \cos \left(\frac{\pi}{4}\right) k+\cos \left(\frac{\pi}{2}\right) k+\frac{1}{2} \cos \left(\frac{3 \pi}{4}\right) k$ | 6 | 4 | 3 | 2.1.2 |
| 6b | $x(n)=\{4,-2,1,0,-2,-3,1,5,-1\}$ <br> Let be a sequence with DTFT $X\left(e^{j \Omega}\right)$. Evaluate the following functions of $X\left(e^{j \Omega}\right)$ without computing $X\left(e^{j \Omega}\right)$. <br> a) $X\left(e^{j 0}\right)$ b) $X\left(e^{j \pi}\right)$ c) $\int_{-\pi}^{\pi} X\left(e^{j \Omega}\right) d \Omega$ <br> d) $\left.\int_{-\pi}^{\pi}\left\|X\left(e^{j \Omega}\right)\right\|^{2} d \Omega e\right) \int_{-\pi}^{\pi}\left\|\frac{d X\left(e^{j \Omega}\right)}{d \Omega}\right\|^{2} d \Omega$ | 8 | 3 | 3 | 1.1.3 |
| 6 c | Obtain the impulse response of the system described by the following equation $\frac{d^{2} y(t)}{d t^{2}}+3 \frac{d y(t)}{d t}+2 y(t)=2 x(t)+\frac{d x(t)}{d t}$ | 6 | 3 | 3 | 1.1.3 |
| UNIT III |  |  |  |  |  |
| 7 a | Prove the following with respect to Z-Transforms <br> a) Initial Value theorem <br> b) Time shift <br> c) ROC of an finite non-causal sequence is entire $Z$-plane except $Z=\infty$ | 10 | 3 | 2 | 1.1.3 |
| 7b | Find the Z-Transform of the following sequences and estimate the ROC <br> a) $x(n)=3^{n+1} u(n)-2(1 / 2)^{n} u(-n-1)$ | 10 | 3 | 3 | 1.1.3 |


| Q.No | Questions | Marks | CO | BL | PI |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | b) $x(n)=3 e^{-2 n} u(n)+2\left[4^{n} u(-n-1)\right]+5 \delta(n)$ <br> c) $x(n)=2 \delta(n-3)-2 \delta(n+3)$ |  |  |  |  |
| 8 a | Calculate the Inverse Z-Transform of <br> $X(Z)=\frac{Z^{3}+Z^{2}+\frac{3}{2} Z+\frac{1}{2}}{Z^{3}+\frac{3}{2} Z^{2}+\frac{1}{2} Z} R O C\|Z\|<\frac{1}{2}$ | 10 | 3 | 3 | 1.1 .3 |
| 8 b | Find the impulse response of the system described by the difference equation <br> $y(n)-\frac{1}{2} y(n-1)=2 x(n-1)$ | 10 | 4 | 3 | 2.1 .2 |

## Blooms Level wise Marks <br> Distrbution



Course Outcome wise Marks Distribution


BL - Bloom's Taxonomy Levels (1- Remembering, 2- Understanding, 3 - Applying, 4 -
Analysing, 5 - Evaluating, 6 - Creating)
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